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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BRADLEY, MATTHEW A	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/722,884	IYER, RAVISHANKAR R.	
	Examiner	Art Unit	
	Matthew Bradley	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-10,14-19,23-26 and 30* is/are rejected.

7)☒ Claim(s) *4-6,11-13,20-22 and 27-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 22 December 2003 was filed after the filing date of 26 November 2003 for application 10/722,884. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner is considering the information disclosure statement with a signed and initialed copy being attached hereto.

Claim Status

Claims 1-30 remain pending and are ready for examination.

Specification

The disclosure is objected to because of the following informalities:

- Paragraph 0002: "For example, a first-level unified (L1) cache may on the same chip as the processor." The verb is missing after the word may.
- Paragraph 0002: "the processor first looks its"

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Appropriate correction is required.

Claim Objections

Claims 1-30 are objected to for the following reasons.

As per claims **1-30**, the Examiner notes that the specification on page 5 paragraph 0016 states that the highest priority requests can be given an allocation

probability number of 100. Further, the specification states that the random numbers are generated from zero (0) to one hundred (100). As per the specification, when the comparison between the randomly-generated number and the allocation probability number takes place, if the randomly-generated number is greater than the allocation probability number, then the allocation takes place. If such is the case, the highest priority requests or the requests that will receive an allocation probability of 100, will never get an allocation. This is so because even considering the highest random number, 100, is generated upon comparison for the highest priority requests, the allocation criteria set forth stating that the allocation probability, 100, has to be greater than the random number, will never be satisfied. Thus bypassing all highest priority requests.

As per dependent claims **5**, **12**, **21**, and **28**, the Examiner notes that the specification on page 5 paragraph 0016 states that, 'If the AP is ***greater*** than the random number, then the cache controller ***allows allocation*** of the cache lines to the requesting thread. On the other hand, if the AP is ***less than or equal to*** the random number, the cache controller ***denies the allocation*** of cache lines...' The instant claims recite, '... ***the allocate condition*** in response to the allocation probability being ***greater than or equal to*** at least one of a ...'

The disclosure clearly relies on the allocation probability number to only be ***greater*** than the random number in order for the allocate condition to exist. However, the claims as written, allow for allocation when the allocation probability number is not only ***greater*** but also when it is ***equal*** to the random number. Accordingly, no explicit

operation can be realized when an equal to condition exists and as such, claims 5, 12, 21, and 28, are objected to.

For examination purposes and in summary, however, the Examiner is interpreting the applicant's to have meant what is instantly claimed. Doing so, allows the highest priority requests to receive allocation, although this contradicts what is clearly recited in the specification this interpretation is necessary in order for the invention to be realized.

As per dependent claim **28**, the phrase 'in response to in response' appears.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-3, 7, 16-19, 23-26, and 30 are rejected under 35 U.S.C. 102(a) and 35 U.S.C. 102(e) as being anticipated by Harris (U.S. 6,601,151).

As per independent claim **1**, Harris teaches,

- assigning a priority level to a cache allocation request; (Column 3 lines 18-24)
- identifying an allocation probability associated with the cache allocation request based on the priority level; and (Column 5 lines 26-30 and Column 7 lines 23-30). *The Examiner notes that Harris teaches determining the likelihood that any given memory access request can be worked upon efficiently in the data storage element at the time. This likelihood is interpreted to be a probability as in if the system determines that there is a high likelihood that the data can worked on, the request would subsequently be reordered in a position to achieve allocation. Accordingly, Harris teaches determining a likelihood which anticipates the instant limitation of probability.*
- identifying the cache allocation request with one of an allocate condition and a bypass condition based on the allocation probability (Column 2 lines 31-41). *The Examiner notes that the transmission of a memory access request to the data storage element as taught by Harris anticipates the instant limitation of identifying the allocation request with one of an allocation condition.*

As per dependent claim **2**, Harris teaches, wherein assigning the priority level to the cache allocation request comprises assigning the priority level to the cache allocation request based on at least one of stream type, source type, and a cache occupancy map (Column 3 lines 18-24).

As per dependent claim **3**, Harris teaches, wherein assigning a priority level to the cache allocation request comprises assigning a priority level to at least one of a cache allocation request associated with a primary host application, a cache allocation request associated with a secondary host application, and a cache allocation request associated with a peripheral application (Column 6 lines 60-64). *The Examiner notes that the processor as taught by Harris contains threads. These threads are as a result of an application running on a processor. Accordingly, the thread is a primary host application making a request as instantly claimed.*

As per dependent claim **7**, Harris teaches,

- further comprising allocating a portion of a cache to the cache allocation request in response to identifying the cache allocation request with the allocate condition and (Column 2 lines 31-41)
- denying the cache allocation request in response to identifying the cache allocation request with the bypass condition (Column 6 lines 19-24).

As per independent claim **16**, Harris teaches,

- a cache to store one or more data blocks of cache allocation requests;(Column 5 lines 21-26). *The Examiner notes that not only does Harris teach a source that is requesting memory that would have storage*

for the request, but the RHU also queues, and thereby stores the allocation requests.

- a priority assignment unit to assign a priority level to a cache allocation request; and (Column 3 lines 18-24)
- a cache controller to identify an allocation probability associated with the cache allocation request based on the priority level, and to identify the cache allocation request with one of an allocate condition and a bypass condition based on the allocation probability (Column 5 lines 26-30 and Column 7 lines 23-30). *The Examiner notes that Harris teaches determining the likelihood that any given memory access request can be worked upon efficiently in the data storage element at the time. This likelihood is interpreted to be a probability as in if the system determines that there is a high likelihood that the data can worked on, the request would subsequently be reordered in a position to achieve allocation. Accordingly, Harris teaches determining a likelihood which anticipates the instant limitation of probability. Further, the RHU of Harris anticipates the controller as instantly claimed.*

As per dependent claim **17**, Harris teaches, wherein the cache allocation request comprises at least one of a cache allocation request associated with a primary host application, a cache allocation request associated with a secondary host application, and a cache allocation request associated with a peripheral application (Column 6 lines 60-64). *The Examiner notes that the processor as taught by Harris contains threads.*

These threads are as a result of an application running on a processor. Accordingly, the thread is a primary host application making a request as instantly claimed.

As per dependent claim **18**, Harris teaches, wherein the priority assignment unit comprises at least one of an operating system, a compiler, and an application specific integrated circuit (Column 3 lines 18-24). *The Examiner notes that a source requesting memory as taught by Harris is the operating system.*

As per dependent claim **19**, Harris teaches, wherein the cache controller is to assign the priority level to the cache allocation request based on at least one of stream type, source type, and a cache occupancy map (Column 3 lines 18-24).

As per dependent claim **23**, Harris teaches, wherein the cache controller is to allocate a portion of the cache to the cache allocation request in response to identifying the cache allocation request with the allocate condition (Column 2 lines 31-41). *The Examiner notes that the transmission of a memory access request to the data storage element as taught by Harris anticipates the instant limitation of identifying the allocation request with allocation condition.*

As per independent claim **24**, Harris teaches,

- a static random access memory (SRAM) to store one or more data blocks of cache allocation requests; and (Column 6 lines 11-18)
- a processor coupled to the SRAM, the processor to: assign a priority level to a cache allocation request; (Figure 7 item 110)
- identify an allocation probability associated with the cache allocation request based on the priority level; and (Column 5 lines 26-30 and

Column 7 lines 23-30). *The Examiner notes that Harris teaches determining the likelihood that any given memory access request can be worked upon efficiently in the data storage element at the time. This likelihood is interpreted to be a probability as in if the system determines that there is a high likelihood that the data can worked on, the request would subsequently be reordered in a position to achieve allocation. Accordingly, Harris teaches determining a likelihood which anticipates the instant limitation of probability.*

- identify the cache allocation request with one of an allocate condition and a bypass condition based on the allocation probability (Column 2 lines 31-41). *The Examiner notes that the transmission of a memory access request to the data storage element as taught by Harris anticipates the instant limitation of identifying the allocation request with one of an allocation condition.*

As per dependent claim **25**, Harris teaches, wherein the cache allocation request comprises at least one of a cache allocation request associated with a primary host application, a cache allocation request associated with a secondary host application, and a cache allocation request associated with a peripheral application (Column 6 lines 60-64). *The Examiner notes that the processor as taught by Harris contains threads. These threads are as a result of an application running on a processor. Accordingly, the thread is a primary host application making a request as instantly claimed.*

As per dependent claim **26**, Harris teaches, wherein the processor is to assign the priority level to the cache allocation request based on at least one of stream type, source type, and a cache occupancy map (Column 3 lines 18-24).

As per dependent claim **30**, Harris teaches, wherein the processor is to allocate a portion of the SRAM to the cache allocation request in response to identifying the cache allocation request with the allocate condition (Column 2 lines 31-41). *The Examiner notes that the transmission of a memory access request to the data storage element as taught by Harris anticipates the instant limitation of identifying the allocation request with an allocation condition.*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 8-10 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rubinstein, (U.S. 5,913,215) herein after referred to as Rubinstein.

Harris does not expressly teach that a method is performed by a software series of instructions, instead disclosing a set of hardware components.

Rubinstein teaches on Column 10 lines 3-15 that computer methods may be performed either by a series of instructions, or by specific hardware components that contain hard-wired logic for performing the method, or by any combination of the two.

Harris and Rubinstein are analogous art because they are from the same general

field of endeavor, namely computer-controlled methods.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the apparatus of Harris by embodying it in executable instructions.

The motivation for doing so is portability and ease of installation. For example, it is well known that a method encoded in a program may be installed onto different systems much more quickly and easily than can hardware components designed to perform the same method.

Therefore, it would have been obvious to combine Harris with Rubinstein for the benefits shown above, to obtain the invention as specified in claims 8-10 and 14-15.

As per independent claim **8**, Harris teaches,

- assign a priority level to a cache allocation request; (Column 3 lines 18-24)
- identify an allocation probability associated with the cache allocation request based on the priority level; and (Column 5 lines 26-30 and Column 7 lines 23-30). *The Examiner notes that Harris teaches determining the likelihood that any given memory access request can be worked upon efficiently in the data storage element at the time. This likelihood is interpreted to be a probability as in if the system determines that there is a high likelihood that the data can worked on, the request would subsequently be reordered in a position to achieve allocation.*

Accordingly, Harris teaches determining a likelihood which anticipates the instant limitation of probability.

- identify the cache allocation request with one of an allocate condition and a bypass condition based on the allocation probability (Column 2 lines 31-41). *The Examiner notes that the transmission of a memory access request to the data storage element as taught by Harris anticipates the instant limitation of identifying the allocation request with one of an allocation condition.*

As per dependent claim **9**, Harris teaches, wherein the instructions, when executed, cause the machine to assign a priority level to the cache allocation request by assigning the priority level to the cache allocation request based on at least one of stream type, source type, and a cache occupancy map (Column 3 lines 18-24).

As per dependent claim **10**, Harris teaches, wherein the instructions, when executed, cause the machine to assign the priority level to the cache allocation request by assigning a priority level to at least one of a cache allocation request associated with a primary host application, a cache allocation request associated with a secondary host application, and a cache allocation request associated with a peripheral application (Column 6 lines 60-64). *The Examiner notes that the processor as taught by Harris contains threads. These threads are as a result of an application running on a processor. Accordingly, the thread is a primary host application making a request as instantly claimed.*

As per dependent claim **14**, Harris teaches, wherein the instructions, which when executed, cause the machine to

- allocate a portion of a cache to the cache allocation request in response to identifying the cache allocation request with the allocate condition, and (Column 2 lines 31-41)
- to deny the cache allocation request in response to identifying the cache allocation request with the bypass condition (Column 6 lines 19-24).

As per dependent claim **15**, Harris teaches, wherein the machine readable medium comprises one of a programmable gate array, application specific integrated circuit, erasable programmable read only memory, read only memory, random access memory, magnetic media, and optical media (Column 12 lines 15-19).

Allowable Subject Matter

Claims **4-6** are objected to as being dependent upon rejected base claim **1**, claims **11-13** are objected to as being dependent upon rejected base claim **8**, claims **20-22** are objected to as being dependent upon rejected base claim **16**, claims **27-29** are objected to as being dependent upon rejected base claim **24**, but would be allowable if rewritten in correct and independent form including all of the limitations of the respective base claims and any intervening claims.

The following is an Examiner's statement of reasons for allowance: the prior art teaches the assignment of a priority level to an allocation request as well as assigning a probability to the request, but fails to teach the combination including the limitation of:

(Claim **4**) "...comprises comparing the allocation probability with at least one of a randomly-generated number and a predetermined number.";

(Claim **5**) "...in response to the allocation probability being greater than or equal to at least one of a randomly-generated number and a pre-determined number.";

(Claim **6**) "...in response to the allocation probability being less than at least one of randomly-generated number and a predetermined number.";

(Claim **11**) "...comparing the allocation probability with at least one of a randomly-generated number and a predetermined number.";

(Claim **12**) "...in response to the allocation probability being greater than or equal to as least one of a randomly-generated number and a pre-determined number.";

(Claim **13**) "...in response to the allocation probability being less than at least one of randomly-generated number and a pre-determined number.";

(Claim **20**) "...is to compare the allocation probability with at least one of a randomly-generated number and a predetermined number.";

(Claim **21**) "...in response to the allocation probability being greater than or equal to at least one of a randomly-generated number and a pre-determined number.";

(Claim **22**) "...in response to the allocation probability being less than at least one of randomly-generated number and a pre-determined number.";

(Claim **27**) "...is to compare the allocation probability with at least one of a randomly-generated number and a predetermined number.";

(Claim **28**) "...in response to the allocation probability being greater than or equal to at least one of a randomly-generated number and a pre-determined number.";

(Claim **29**) "...in response to the allocation probability being less than at least one of randomly-generated number and a pre-determined number."

If the applicant should choose to rewrite the independent claims to include the limitations recited in the dependent claims, the applicant is then encouraged to amend the title of the invention such that it is descriptive of the invention as claimed, as required by sec. 606.01 of the MPEP. Furthermore, the summary of the invention and the abstract should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of sec. 1302.01 of the MPEP.

As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the MPEP.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. U.S. Patent 6,857,046 Batcher teaches cache allocation based on priority.

2. U.S. Patent 5,983,313 Heisler et al teach allocation based on the probability of demand.

3. U.S. Patent 5,875,464 Kirk teaches cache allocation based on priority.

4. U.S. Patent 5,539,893 Thompson et al teach an allocation method based off priority.

5. U.S. Patent Application Publication 2004/0193827 Mogi et al teach an allocation method based on priority.

6. U.S. Patent Application Publication 2003/0154112 Neiman et al teach a system and method to allocate computer resources.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Bradley whose telephone number is (571) 272-8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DAS/mb

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